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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,439	09/30/2003	Douglas D. Coolbaugh	BUR920020094US1	2438

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,439	COOLBAUGH ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,4-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/17/2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4, 6-7, 9, 11-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kadosh et al (US 6,069,398)

Kadosh discloses a method for forming a thin film polysilicon resistor. The method comprises the steps of:

providing a structure that includes at least one polysilicon resistor device region 30 and at least one other type of device region, said at least one polysilicon resistor device region comprising a polysilicon layer (col 4, lines 44-46; col 10, lines 10-13)

selectively performing an ion implant in the at least one other type of device region (col 6, lines 38-48), forming one polysilicon gate of a MOSFET (col 4, lines 44-47), using a rapid thermal annealing to anneal the silicon wafer/other type of device region (col 8, lines 28-31)

subsequently, forming a protective dielectric layer 130 covering the polysilicon layer in the polysilicon resistor device region (col 8, lines 41-44; fig. 2E)

subsequently, doping the polysilicon with dopants to select value of resistance of the fabricated resistor (col 9, lines 20-38, abstract), which reads on providing a predetermined resistance value to the polysilicon layer in the polysilicon resistor device region

Regarding claim 2, Kadosh discloses one polysilicon device region comprises a semiconductor substrate, the polysilicon layer located on the substrate and a dielectric layer 130 located on the polysilicon layer (col 8, lines 40-45; fig. 2F)

Regarding claim 4, Kadosh discloses forming a patterned photoresist 26 atop the at least one polysilicon resistor device region to protect the region during said selective ion implant (fig. 6)

The limitation of claim 6 has been discussed above

Regarding claim 7, Kadosh discloses implanting with n-type or p-type dopant to select the value of resistance (col 9, lines 20-22)

Regarding claim 9, Kadosh discloses performing an annealing step after the step of doping to select the value of resistance (col 4, lines 45-48)

Regarding claim 11, Kadosh discloses exposing end portions of the polysilicon layer (Fig. 2H)

Regarding claims 12-13, Kadosh discloses performing a silicidation process to form silicide contact on the exposed polysilicon (col 9, lines 40-45)

Regarding claim 14-16, Eklund discloses forming a conductive layer of Ti and performing an anneal to cause reaction of the Ti with the polysilicon layer to form silicide (col 11, lines 20-25)

4. Claims 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kadosh et al (US 6,069,398)

Kadosh discloses a method for forming a thin film polysilicon resistor. The method comprises the steps of:

performing a rapid thermal annealing on a structure that includes at least one partially polysilicon resistor device region 30 and at least one other type of device region (col 8, lines 28-31), the polysilicon resistor having a polysilicon layer (col 4, lines 1-10), forming one polysilicon gate of a MOSFET (col 4, lines 44-47)

subsequently, forming a protective dielectric layer covering the polysilicon layer in the polysilicon resistor device region to protect the polysilicon layer (col 8, lines 41-44; fig. 2E)

subsequently, ion implanting a dopant into the polysilicon layer through the dielectric layer (col 9, lines 20-30; fig. 2H)

subsequently, performing silicide processing to form the polysilicon resistor (col 9, lines 41-45)

Regarding claims 18-19, Kadosh discloses performing a thermal anneal in combination with the silicidation step (col 9, lines 46-48)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadosh et al (US 6,069,398)

Kadosh method has been described above. Kadosh differs from the instant claimed inventions as per claims 5, 20 by forming a protective dielectric layer 130 of silicon dioxide instead of nitride. However, Kadosh also discloses using silicon dioxide or silicon nitride as a protective/spacer layer (col 6, lines 62-64)

One skilled in the art at the time the invention was made would have found it obvious to substitute Kadosh silicon dioxide layer 130 with silicon nitride because Kadosh discloses that silicon nitride films serve as mechanical protective layer for integrated circuit and are suitable for usage as a passivation layer by acting as a nearly impervious barrier to diffusion (col 7, lines 1-6)

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadosh et al (US 6,069,398) in view of Gardner et al (US 6,027, 964)

Kadosh method has been described above. Unlike the instant claimed invention as per claim 8, Kadosh fails to specifically disclose that the ion implantation provides the polysilicon layer with a dopant concentration of from about $1x10^{14}$ to about $1x10^{21}$ atom/cm3.

Gardner discloses a method for making an FET comprises the step of the ion implanting the polysilicon layer with a dopant concentration of from about $1x10^{15}$ atom/cm3 (col 6, lines 40-41)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Kadosh method by implanting the polysilicon layer with a dopant concentration as per Gardner because Gardner discloses that the polysilicon can be doped by implanting with a dosage in the range of $1x10^{15}$ to about $5x10^{15}$ atoms/cm3 (col 6, lines 38-40)

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadosh et al (US 6,069,398) in view of Segawa et al (US 6,436,747)

Kadosh method has been described above. Unlike the instant claimed invention as per claim 10, Kadosh fails to specifically disclose that the annealing step is performed in an inert gas ambient that may optionally be mixed with less than about 10% oxygen

Segawa discloses a method for fabricating semiconductor device comprises the step of annealing the polysilicon in nitrogen/inert gas and oxygen (col 8, lines 39-44)

Thus, one skilled in the art at the time the invention was made would have found it obvious to modify Kadosh method by annealing the polysilicon in nitrogen/inert gas and oxygen as per Segawa because according to Segawa, the out-diffusion of the n-type impurity is suppressed during the RTA process containing oxygen (col 11, lines 4-7)

Response to Arguments

9. Applicant's arguments, filed on 12/16/2005 with respect to claims 1-2, 4-20 have been considered but are moot in view of the new ground(s) of rejection. The applicants argue that none of the cited reference teaches or suggest a method comprising processing steps that are carried out the claimed sequence. This argument is moot in view of the new ground of rejection based on newly cited reference of Kadosh et al (US 6,069,398) that discloses a method comprising processing steps that are carried out in the claimed sequence

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
January 31, 2006